an analog/digital converting section for receiving relevant picture data signals of R, G and B data signals, respectively, of the first video signals from said OSD generating section so as to convert them to digital signals;

a buffering section for receiving and storing the picture data signals from said analog/digital converting section, and for outputting previous picture data signals upon receiving next picture data signals from said analog/digital converting section;

a pivot controller for outputting storing position control signals and data selection control signals in response to the pivot control signals of said control section;

a data storing section for receiving and storing the picture data signals of said buffering section, and for storing in a position-converting manner a write address of the picture data signals of said buffering section in correspondence with the pre-set pivot write address in response to the storing position control signals; and

a data selector for receiving one of the picture data signals of the first video signals and the picture data signals of said data storing section, and for outputting said one of the picture data signals of the first video signals and the picture data signals of said data storing section in a form of second video signals.

4. The video display apparatus as claimed in claim 3, wherein said buffering section comprises eight buffers for storing 8-bit picture data signals from said analog/digital converting section.

5. A video display apparatus with an on-screen display pivoting function, comprising:

a power supply section for supplying power;

a display section for receiving the power from said power supply section, and for displaying a picture of externally inputted video signals to a user;

a signal converter/clock generator section for receiving horizontal/vertical synchronizing signals and video signals, for converting the video signals to first digital signals in response to first control signals, and for generating clock signals;

a decoder for receiving brightness/chromatic signals, and for converting the brightness/chromatic signals to second digital signals in response to second control signals;

a frame rate converter section for receiving the horizontal/vertical synchronizing signals and the video signals from said signal converter/clock generator section, for receiving the brightness/chromatic signals from said decoder, for storing the video signals in response to third control signals, and for converting the stored video signals so as to have a certain frequency ratio in correspondence with display characteristics of the display section;

an on-screen display (OSD) generating section for receiving the horizontal/vertical synchronizing signals and the clock signals, and for outputting first video signals in response to OSD control signals;

a pivot circuit section for receiving the first video signals, for storing in a position-converting manner a write address of the first video signals in correspondence with a pre-set pivot write address, and for converting the write address in response to the horizontal/vertical synchronizing signals and the clock signals so as to output the first video signals in the form of second video signals;

a scale converting section for furnishing the horizontal/vertical synchronizing signals and the clock signals to said OSD generating section and said pivot circuit section, respectively, for converting scales of video signals of said frame rate converting section, and for receiving the second video signals so as to convert scales of the second video signals of said pivot circuit section in response to scale control signals;

a control section for furnishing the first, second and third control signals to said signal converting/clock generating section, said decoder and said frame rate converting section, respectively, for furnishing the OSD control signals and the scale control signals to said OSD generating section and said scale converting section, respectively, in response to OSD driving signals, and for furnishing pivot control signals to said pivot circuit section in response to mode control signals; and

a driving section for furnishing video signals and driving signals from said scale converting section to said display section.

6. The video display apparatus as claimed in claim 5, wherein said pivot circuit section comprises:

an R-pivot circuit for receiving R-data signals of the first video signals from said OSD generating section, for storing in a position-converting manner a write address of the R-data signals in correspondence with a pre-set pivot write address in response to the pivot control signals, and for converting the write address in response to the horizontal/vertical synchronizing signals and the clock signals so as to output the stored R-data signals in a form of R-data signals of the second video signals;

a G-pivot circuit for receiving G-data signals of the first video signals from said OSD generating section, for storing in a position-converting manner a write address of the G-data signals in correspondence with the pre-set pivot write address in response to the pivot control signals, and for converting the write address in response to the horizontal/vertical synchronizing signals and the clock signals so as to output the stored G-data signals in a form of G-data signals of the second video signals; and

a B-pivot circuit for receiving B-data signals of the first video signals from said OSD generating section, for storing in a position-converting manner a write address of the B-data signals in correspondence with the pre-set pivot write address in response to the pivot control signals, and for converting the write address in response to the horizontal/vertical synchronizing signals and the clock signals so as to output the stored B-data signals in a form of B-data signals of the second video signals.

7. The video display apparatus as claimed in claim 6, wherein each of said R, G and B pivot circuits comprises:

an analog/digital converting section for receiving relevant picture data signals of the R, G and B data signals, respectively, of the first video signals from said OSD generating section so as to convert them to digital signals;

a buffering section for receiving and storing the picture data signals from said analog/digital converting section, and for outputting previous picture data signals upon receiving next picture data signals from said analog/digital converting section;

a pivot controller for outputting storing position control signals and data selection control signals in response to the pivot control signals of said control section;

a data storing section for receiving and storing the picture data signals of said buffering section, and for storing in a position-converting manner a write address of the picture data signals of said buffering section in correspondence with a pre-set pivot write address in response to store position control signals; and

a data selector for receiving one of the picture data signals of the first video signals and the picture data signals of said data storing section, and for outputting said one of the picture data signals of the first video signals and the picture data signals of said data storing section in a form of second video signals.

8. The video display apparatus as claimed in claim **7**, wherein said buffering section comprises eight buffers for storing 8-bit picture data signals from said analog/digital converting section.

9. The video display apparatus as claimed in claim **5**, wherein said frame rate converter section comprises:

a frame memory for storing the digital video signals from said signal converter/clock generator section in response to control inputs; and

a frame rate converter for writing the output video signals of said signal converter/clock generator section into said frame memory, and for reading out the video signals written into said frame memory so as to convert the video signals to have a certain frequency ratio in correspondence with display characteristics of said display section.

10. The video display apparatus as claimed in claim **9**, wherein said frame rate converter generates said control inputs and provides said control inputs to said frame memory.

11. The video display apparatus as claimed in claim **5**, wherein said OSD driving signals are generated by the user.

12. The video display apparatus as claimed in claim **5**, wherein said mode control signals are generated by the user.

13. A video display apparatus having an on-screen display pivoting function, comprising:

on-screen display (OSD) generating means for outputting first video signals having a write address in response to OSD control signals;

pivot circuit means for receiving the first video signals, for converting the write address of the first video signals, and for outputting the first video signal in a form of second video signals having scales;

scale converting means for receiving the second video signals and for converting the scales of the second video signals in response to scale control signals; and

control means for furnishing the OSD control signals and the scale control signals to said OSD generating means and said scale converting means, respectively, in response to OSD driving signals generated by a user input.

14. The video display apparatus as claimed in claim **13**, wherein said pivot circuit means comprises:

an R-pivot circuit for receiving R-data signals of the first video signals from said OSD generating means, for storing a write address of the R-data signals in response to pivot control signals generated by said control means, and for converting the write address so as to output the R-data signals in a form of R-data signals of the second video signals;

a G-pivot circuit for receiving G-data signals of the first video signals from said OSD generating means and for converting the write address so as to output the stored G-data signals in a form of G-data signals of the second video signals; and

a B-pivot circuit for receiving B-data signals of the first video signals from said OSD generating means and for converting the write address so as to output the stored B-data signals in a form of B-data signals of the second video signals.

15. The video display apparatus as claimed in claim **14**, wherein each of said R,G and B pivot circuits comprises:

an analog/digital converting section for receiving relevant picture data signals of R,G and B data signals, respectively, of the first video signals from said OSD generating means so as to convert them to digital signals;

a buffering section for receiving and storing the picture data signals from said analog/digital converting section, and for outputting previous picture data signals upon receiving next picture data signals from said analog/digital converting section;

a pivot controller for outputting storing position control signals and data selection control signals in response to pivot control signals from said control means;

a data storing section for receiving and storing the picture data signals of said buffering section, and for storing a write address of the picture data signals of said buffering section in response to the storing position control signals; and

a data selector for receiving one of the picture data signals of the first video signals and the picture data signals of said data storing section, and for outputting said one of the picture data signals of the first video signals and the picture data signals of said data storing section in a form of second video signals.

16. The video display apparatus as claimed in claim **15**, wherein said buffering section comprises eight buffers for storing 8-bit picture data signals from said analog/digital converting section.

17. The video display apparatus as claimed in claim **13**, further comprising:

signal converting/clock generating means for receiving horizontal/vertical synchronizing signals and video signals, for converting the video signals to first digital signals in response to first control signals from said control means, and for generating clock signals.

18. The video display apparatus as claimed in claim **17**, further comprising:

decoder means for receiving brightness/chromatic signals, and for converting the brightness/chromatic signals to second digital signals in response to second control signals from said control means.

19. The video display apparatus as claimed in claim **18**, further comprising:

frame rate converting means for receiving the horizontal/vertical synchronizing signals and the first video signals from said signal converting/clock generating means, for receiving the brightness/chromatic signals from said decoder means, for storing the first video signals in response to third control signals from said control means, and for converting the stored first video signals so as to have a certain frequency ratio in correspondence with display characteristics of a display section.

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